1. Scope :

This specification applies to NPN silicon phototransistor chips,
Device No. ST-0124.

2. Structure :

2-1. Planar type.
2-2. Electrodes :
N (Collector) side : Gold alloy.
P (Base) side : Aluminum alloy.
N (Emitter) side : Aluminum alloy.

3. Size :

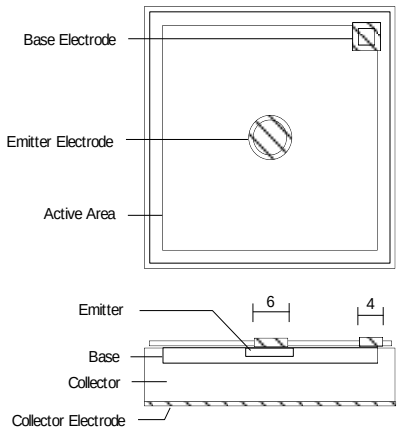
3-1. Chip size : 24 mils × 24 mils (0.610 mm × 0.610 mm).
3-2. Chip thickness : 7.0 ± 1.2 mils (0.178 ± 0.03 mm).
3-3. Active area : 17 mils × 17 mils ± 1.2 mils (0.432 mm × 0.432 mm ± 0.03 mm).
3-4. Bonding pad diameter: 5 mils ± 0.8 mils (0.125 mm ± 0.02 mm).
3-5. Pattern drawing : refer to the attached drawing.

*Including scribing line .The chip size is about (0.585±0.025)×(0.585± 0.025)mm^2 after dicing.

4. Electrical characteristics (Ta = 25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Collector-emitter Breakdown Voltage	BV_{CEO}	I_C=100μA I_B=0	30		100	V
Emitter-collector Breakdown Voltage	BV_{ECO}	I_E=100μA I_B=0	6.5			V
Collector dark current	I_{CEO}	VCE=20V H=0mw/cm^2			100	nA
Collector-emitter Saturation Voltage	$V_{CE(S)}$	Ic=2mA I_B=100uA			0.2	V
Rise/fall time	t_R/t_F	VCE=5V IC=1mA R_L=1000Ω		15/15		μS
Current gain	h_{FE}	VCE=5V I_C=2mA	200			
Collector-base Capacitance	C_{CB}	f=1MHZ V_{CB}=3V	5.4	6.4	7.4	PF

PATTERN DRAWING
UNIT:mil



*1 hFE rank table.

Rank	Chip Spec. hFE range	
	MIN	MAX
A	200	400
B	350	700
C	700	1050
D	1000	1800

When hFE range MAX (wafer test) is 1000 or more, the MIN of the BVECO is 3 V