1. Scope :

This specification applies to NPN silicon phototransistor twin Chips,
Device No. ST-0122

2. Structure :

2-1. Planar type.
2-2. Electrodes :
N (Collector) side : Gold alloy.
P (Base) side : Aluminum alloy, PAD thickness:2.25um ± 0.3um.
N (Emitter) side : Aluminum alloy, PAD thickness:2.25um ± 0.3um.

3. Size :

3-1. Chip size : 18 mils × 48 mils (0.457 mm × 1.220 mm).
3-2. Real chip size : 17 mils × 47 mils ± 1 mils (0.432 mm × 1.195 mm ± 0.025 mm).
3-3. Chip thickness : 7.0 ± 1.5 mils (0.178 ± 0.038 mm).
3-4. Active area : 12.6 mils × 18.6 mils (0.320 mm × 0.472 mm).
3-5. Pattern drawing : refer to the attached drawing.

4. Electrical characteristics (Ta = 25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Collector-emitter Breakdown Voltage	BV_{CEO}	I_C=100uA I_B=0	30			V
Emitter-collector Breakdown Voltage	BV_{ECO}	I_E=100uA I_B=0	5			V
Collector dark current	I_{CEO}	V_{CE}=20V H=0mw/cm²			100	nA
Collector-emitter Saturation Voltage	$V_{CE(S)}$	Ic=2mA IB=100uA			0.3	V
Rise/fall time	t_R/t_F	V_{CE}=5V I_C=1mA R_L=1000Ω		15/15		uS
Current gain	h_{FE}	V_{CE}=5V I_C=2mA	500			

hFE Rank A : 700 - 1400
Rank B : 900 - 1800
Rank C : 1300 - (BVeco：Min=3V)

Pattern drawing